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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/747,621 | 12/30/2003 | Byeong Ryeol Lee | 040008-0307457 | 2865 |

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| EXAMINER | |
|---|---|
| JEFFERSON, QUOVAUNDA | |
| **ART UNIT** | **PAPER NUMBER** |
| 2823 | |

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/747,621 | LEE, BYEONG RYEOL | |
| | Examiner | Art Unit | |
| | Quovaunda Jefferson | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benaissa et al, US Patent Application Publication 2002/0084494 in view of Delgado et al, US Patent 5,959,508 or Chang et al, US Patent 6,069,091. See Benaissa figure below.

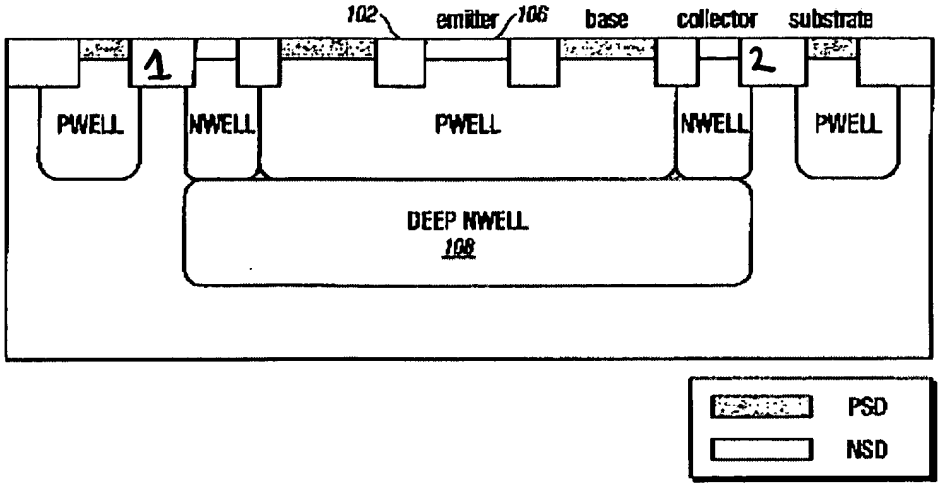


*FIG. 1*
*( PRIOR ART )*

Regarding claim 1, Benaissa teaches a method of forming device isolation structures in an embedded semiconductor device comprising the steps of providing a semiconductor substrate having a first area in which ions are implanted (figure 1. The first area of the substrate is the area where the **DEEP NWELL, PWELL** and **EMITTER** are located), forming a first device isolation region (labeled **1**) in the first area, forming a first type well **108** with deep junction by diffusing the ions in the first area, forming a second device isolation region (labeled **2**) with a trench in a second area of the semiconductor substrate, forming a first type well **NWELL** with shallow junction in peripheral regions of the second device isolation structure **2** and a region between the first device isolation structure **1** and the second device isolation structure **2**, forming a second type well **PWELL** with shallow junction in peripheral regions of the first device

isolation structure **1** and a region of the second device isolation structure **2**, and defining first and second type active regions **PSD and NSD** on the semiconductor substrate.

Benaissa fails to teach forming a device isolation region through partial oxidation. Delgado teaches forming a device isolation region through partial oxidation as a method of forming a stress region that surrounds a gettering trench (column 4, lines 26-30 and figure 8 and column 1, lines 38-41).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Delgado with that of Benaissa in the formation of a gettering trench, which attracts impurities in the substrate, making it beneficial to the substrate.

In addition, Chang teaches forming a device isolation region through partial oxidation as a method of forming an oxide layer within a trench (column 1, lines 48-52).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Chang with that of Benaissa because the partial oxidation of a trench isolation region forms an oxide liner in the trench, which can smooth out the profile of a jagged-edge trench after formation of the trench through etching.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Chu with that of Benaissa because the thermal oxidation of the trench wall to form a liner oxide in a device isolation trench is conventionally technique that is known in the art.

Regarding claim 3, Benaissa further teaches the first type well is an n-type well and the second type well is a p-type well (figure 1 above).

### *Allowable Subject Matter*

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Regarding claim 2, prior art fails to teach the diffusion of ions is simultaneously conducted when the partial oxidation is performed.

### *Response to Arguments*

Applicant's arguments, see page 3, filed May 10th, 2006, with respect to the rejection(s) of claim(s) 1-3 under 35 USC 102(b) have been fully considered and are

persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found art.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 4,954,456, issued to Kim et al, discloses fabrication for high speed and high packing density semiconductor device. US Patent 5,024,962, issued to Murray et al, discloses method for preventing auto-doping in the fabrication of metal gate CMOS devices. US Patent 5,637,524, issued to Lee et al, discloses a method for forming wells of semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fernando Toledo
Patent Examiner
Art Unit 2823

QVJ